

Nonpolar-Oriented Wurtzite InP Nanowires with Electron Mobility Approaching the Theoretical Limit

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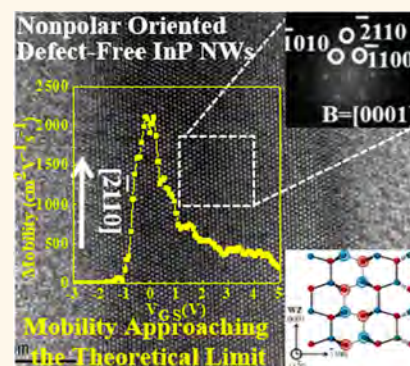
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Supporting Information

ABSTRACT: As an important semiconductor nanomaterial, InP nanowires (NWs) grown with a typical vapor–liquid–solid mechanism are still restricted from their low electron mobility for practical applications. Here, nonpolar-oriented defect-free wurtzite InP NWs with electron mobility of as high as $2000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ can be successfully synthesized via Pd-catalyzed vapor–solid–solid growth. Specifically, PdIn catalyst particles are involved and found to expose their PdIn{210} planes at the InP nucleation frontier due to their minimal lattice mismatch with nonpolar InP{ $\bar{2}110$ } and { $\bar{1}100$ } planes. This appropriate lattice registration would then minimize the overall free energy and enable the highly crystalline InP NW growth epitaxially along the nonpolar directions. Because of the minimized crystal defects, the record-high electron mobility of InP NWs (*i.e.*, $2000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at an electron concentration of 10^{17} cm^{-3}) results, being close to the theoretical limit of their bulk counterparts. Furthermore, once the top-gated device geometry is employed, the device subthreshold slopes can be impressively reduced down to 91 mV dec^{-1} at room temperature. In addition, these NWs exhibit a high photoresponsivity of 10^4 A W^{-1} with fast rise and decay times of 0.89 and 0.82 s, respectively, in photodetection. All these results evidently demonstrate the promise of nonpolar-oriented InP NWs for next-generation electronics and optoelectronics.

KEYWORDS: InP nanowire, nonpolar, electron mobility, vapor–solid–solid, in-plane lattice mismatch



In the past decade, among many III–V compound semiconductor nanomaterials, InP nanowires (NWs) have attracted considerable interest due to their versatility in electronics and optoelectronics. They have been widely explored for applications in field-effect transistors (FETs),^{1,2} photodetectors,^{3–5} terahertz detectors,^{6,7} solar cells,^{8–10} and so on. In most of their utilizations, electron mobility is one of the key performance parameters that receives significant attention in order to pursue high-mobility devices for the “beyond silicon” era.¹¹ However, until now, electron mobility of InP NWs has been demonstrated to be insufficiently low at around only $1000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with an electron concentration of 10^{17} – 10^{18} cm^{-3} ,^{7,12–16} being far below the bulk mobility limit of

$\sim 2000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at the corresponding electron concentration.^{17,18} This relatively low electron mobility is mostly associated with the existence of various defects, such as stacking faults and polytypism, throughout all of the InP NWs.^{19–21} In this regard, synthesizing high-quality InP NWs with excellent electron mobility is urgently required but inevitably remains a substantial technological challenge.

In general, electron mobility of III–V NWs is found to be determined by a combination of factors, such as crystallinity,

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growth orientation, and diameter, *etc.*,^{22–26} especially since acoustic scattering at the surface/bulk defect sites would greatly deteriorate electron motions within the NWs. For example, Johansson *et al.* pointed out that most III–V NWs would grow along the direction of $\langle 111 \rangle_B$; however, this particular NW growth orientation is surprisingly observed to restrict the performance of their subsequently fabricated optoelectronic devices because of the associated defects and inappropriate atomic stacking in the polar $\langle 111 \rangle_B$ direction.²⁷ At the same time, electron mobility would also be degraded considerably when there are abundant stacking faults occurring within the InAs NWs.²³ As a result, many methods have then been developed to control the NW crystallinity, growth orientation, diameter, and such with an aim to minimize the adverse effects of various kinds of crystal/surface defects on the electronic transport properties of NWs.^{28,29} In any case, because of the high surface-to-volume ratio of NWs, both cubic zincblende (ZB) and hexagonal wurtzite (WZ) phases are thermodynamically stable on the nanometer scale, which always leads to the formation of mixed phases with different growth orientations, such as ZB $\langle 111 \rangle$, $\langle 110 \rangle$ and WZ $\langle 0001 \rangle$, even within an individual InP NW catalyzed by Au in the well-established vapor–liquid–solid (VLS) growth.^{12,14,20,30,31} The Au catalyst is notoriously incompatible with the silicon-based complementary metal oxide semiconductor (CMOS) technology.^{32,33} Also, all these crystal defects are known to scatter electrons, leading to the relatively low electron mobility of InP NWs as compared with the theoretical value.

Recently, another NW growth mechanism, namely the vapor–solid–solid (VSS) scheme, has been widely explored as an effective method to control NW synthesis, including the crystal phase, orientation, and diameter, *etc.*^{28,34} In distinct contrast to the VLS growth, in this VSS scheme, a high melting-point metal catalyst is typically adopted where the catalyst would then form alloy nanoparticles with precursor vapors with the eutectic temperature higher than the NW growth temperature, yielding solid-state catalytic seeds during NW nucleation.^{35–37} For instance, Ross *et al.* utilized Cu catalyst particles for the preparation of VSS grown Si NWs.³⁸ In our previous work, high-performance $\langle 111 \rangle$ -oriented GaSb NWs have also been readily obtained through the VSS growth by using CMOS-compatible Pd as the catalyst.²⁸ Employing a similar technique here, pure WZ InP NWs with nonpolar growth orientations of $\langle 2\bar{1}10 \rangle$ and $\langle \bar{1}100 \rangle$ were successfully achieved. To be explicit, during the growth, the immobile polyhedral solid catalyst tips are observed to dictate the NW growth direction following the epitaxy relationship at the seed/NW interface. This epitaxy growth is independent of the NW diameters and synthesis conditions, demonstrating the significant advantage in realizing NWs with controlled crystallographic phase and orientation. More importantly, when constructed into back-gated field-effect transistors (FETs), the as-prepared InP NWs show a peak electron mobility of $\sim 2000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in which this value already approaches the theoretical mobility limit under the corresponding electron concentration of $\sim 10^{17} \text{ cm}^{-3}$. It is also noted that an impressive photoresponsivity of 10^4 A W^{-1} is obtained for the NW photodetector, while an extraordinary subthreshold slope (SS) of 91 mV dec^{-1} is measured for the top-gated NW devices. All of these findings evidently indicate the promise of these high-performance nonpolar InP NWs for a wide range of next-generation electronic and optoelectronic applications.

RESULTS AND DISCUSSION

During typical VLS III–V NW growth, the widely adopted CMOS-incompatible Au catalyst usually yields nonuniform crystal quality, orientation, and other physical properties.^{14,19,39} To tackle these issues, the higher melting temperature catalysts, such as Ni and Pd, *etc.*, were investigated to replace Au in order to enable the VSS NW growth.^{35,40–45} In this work, Pd is purposely selected as the catalyst for the InP NW growth since the melting points of Pd_xIn_y binary alloys are as high as 672–1365 °C,⁴⁶ being far higher than the corresponding NW synthesis temperature of 530 °C, assuring the VSS growth mode. As shown in the scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images (Figure 1a,b), the as-synthesized Pd-catalyzed

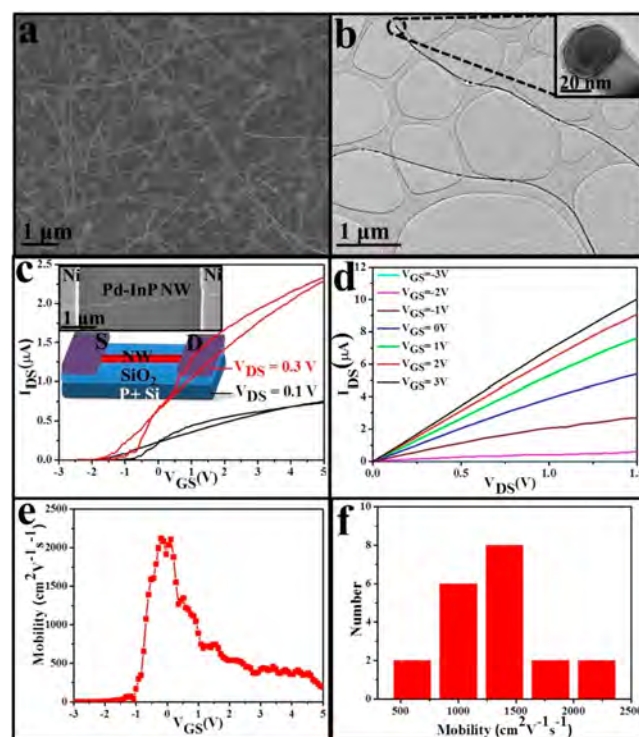


Figure 1. Morphological and electrical characterization of as-prepared InP NWs. (a, b) SEM and TEM images of the as-prepared Pd-catalyzed InP NWs. The inset of (b) is a typical TEM image of an individual InP NW at the tip region. (c, d) $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ characteristics of the Pd-catalyzed InP NW device configured in the global back-gated geometry. SEM image and illustrative schematic of the as-fabricated FET are displayed in the insets of (c). (e, f) Mobility and corresponding statistics of the as-fabricated Pd-catalyzed InP NWFETs.

InP NWs are straight and smooth with length greater than 10 μm . Notably, there is a polyhedral-shaped catalyst seed clearly observed at the tip region of the NW (Figure 1b inset), which is in a distinct contrast to the spherical Au seeds witnessed in other kinds of NW growth, confirming the VSS growth mode again. Importantly, compared to the Au-catalyzed NWs,¹⁴ these Pd-catalyzed InP NWs show a relatively narrow diameter distribution of $35.9 \pm 8.7 \text{ nm}$ (Figure S1), which facilitates the NWs for practical utilizations in nanoscale devices.

Moreover, electrical properties of the as-prepared Pd-catalyzed InP NWs can be further evaluated by fabricating the back-gated NWFETs with different NW channel

Table 1. Comparison of the Synthesis Parameters and the Fundamental Properties of Different Bottom-up InP Nanowires

catalyst	growth mechanism	diameter (nm)	crystal phase	growth orientations	peak mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	conc (cm^{-3})	ref
Au	VLS	~100	ZB		150	3.0×10^{18}	16
Au	VLS	40	ZB/WZ	$\langle 111 \rangle$	350	2.3×10^{18}	14
Au	VLS	100	ZB/WZ		<600	4.6×10^{18}	12
In	VLS	~100	ZB	$\langle 111 \rangle$	922	2×10^{17}	15
No catalyst		240–260	WZ	$\langle 0001 \rangle$	1260		7
Pd	VSS	35	WZ	$\langle \bar{1}100 \rangle$, $\langle \bar{2}110 \rangle$	2000	$2.4 \times 10^{17} - 5.7 \times 10^{17}$	this work

dimensions (Figure 1c–f). Specifically, for the long channel devices with a channel length of $>1 \mu\text{m}$, the intrinsic transport properties (e.g., field-effect electron mobility) can be deduced from the diffusive transport of carriers, removing the effect of ballistic or quasi-ballistic transport. As presented in the $I_{\text{DS}} - V_{\text{GS}}$ curve in Figure 1c, the as-fabricated back-gated FET shows a typical n-type conducting behavior and a decently high $I_{\text{ON}}/I_{\text{OFF}}$ ratio of 10^5 (Figure S2). The $I_{\text{DS}} - V_{\text{DS}}$ curve also confirms the ohmic-like contact formation between the InP NW and the Ni electrodes (Figure 1d). The corresponding electron mobility of NW can then be estimated using a well-established square law model,²³ namely, $\mu = g_{\text{m}}(L^2/C_{\text{ox}})(1/V_{\text{DS}})$, where μ is the mobility, g_{m} is the transconductance at a low bias of 0.1 V, L is the channel length, and C_{ox} is the gate capacitance. The g_{m} can be extracted from the $I_{\text{DS}} - V_{\text{GS}}$ curve (Figure 1c) of the back-gated FETs, following the equation of $g_{\text{m}} = (dI_{\text{DS}})/(dV_{\text{GS}})/V_{\text{DS}}$. The gate capacitance (C_{ox}) can be simulated by software of COMSOL via the finite element analysis (Figure S2). Meanwhile, the electron concentration (n_{h}) of the as-prepared InP NW can also be explicitly calculated by utilizing the equation of $n_{\text{h}} = Q/(q\pi r^2 L) = (C_{\text{ox}} V_{\text{th}})/(q\pi r^2 L)$, where V_{th} is the threshold voltage and r is the radius of NW. The threshold voltage of V_{th} can be estimated easily from the transfer curves (Figure S2). Specifically, for a typical NWFET with a NW of 35 nm in diameter and a $3.5 \mu\text{m}$ in channel length (Figure 1c), the peak electron mobility is found as $\sim 2000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ while the electron concentration is assessed to fall into a range of $(2.4 - 5.7) \times 10^{17} \text{ cm}^{-3}$ due to the observed hysteresis in the transfer curve. It should be noted that this obtained mobility is already approximating the theoretical limit of bulk InP for the electron concentration of 10^{17} cm^{-3} ,^{17,18} which represents a record here among all “bottom-up” InP NWs reported in the literature (Table 1). In order to further assess the overall electrical performance of synthesized NWs, the electron mobilities of more than 20 NWFETs are compiled (Figure 1f). It is obvious that most of the NWs have relatively high electron mobility (i.e., 1000–2000 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), where the slight fluctuation can be attributed to the variation of different NWs in their diameters and surface roughness, etc. Evidently, InP NWs with record-high electron mobility can be readily synthesized by the Pd-catalyzed VSS growth scheme in the conventional CVD system.

To shed light on assessing the origin of these high-performance Pd-catalyzed InP NWs, the growth characteristics of as-prepared NWs are thoroughly investigated by high-resolution TEM (HRTEM) and energy-dispersive X-ray spectroscopy (EDS) (Figure 2). To be explicit, these two Pd-catalyzed InP NWs contain the polyhedral-shaped catalytic tips, which is in a distinct difference to other InP NWs grown with the spherical Au catalyst seeds. The polyhedral-shaped catalyst is found to obtain a stoichiometry of Pd/In = 1:1, while the NW body contains a chemical composition ratio of

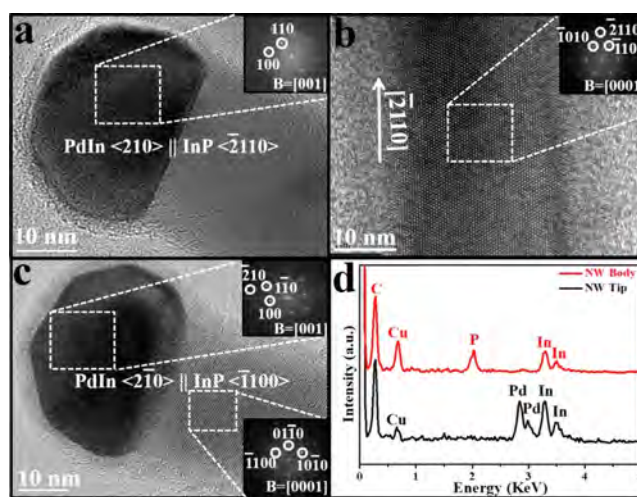


Figure 2. Electron microscopy observation on the representative Pd-catalyzed InP NWs. (a–c) HRTEM images and the corresponding FFT images (inset) of the top and body regions of typical InP NWs. All of the as-prepared Pd-catalyzed InP NWs show the polyhedral-shaped catalyst tips. (d) EDS spectra of the catalyst and body regions of a typical Pd-catalyzed InP NW.

In/P = 1:1 as confirmed by both EDS (Figure 2d) and lattice parameters extracted from the HRTEM and FFT images (Figure 2a–c). It should be noted that the InP NW growth temperature of $530 \text{ }^\circ\text{C}$ is much lower than the PdIn catalyst melting point of $1285 \text{ }^\circ\text{C}$,⁴⁶ verifying again the VSS growth mode. Importantly, the NW body exhibits excellent crystallinity with no observable crystal defects of stacking faults, etc., where this minimized defect concentration (i.e., reduced carrier scattering) would contribute to the excellent electron mobility of NWs witnessed. Furthermore, for most of the NWs investigated, the interface of catalyst/NW is predominantly identified to have the interface in-plane relationship of ZB PdIn $\{210\}$ |WZ InP $\{2110\}$ with the NW body growing along the nonpolar $\langle 2110 \rangle$ directions in the hexagonal WZ crystal phase (Figure 2a, Supporting Information Figure S3). Simultaneously, there is also a small amount of InP NWs (<10%) growing along another nonpolar $\langle 1100 \rangle$ direction with similar polyhedral PdIn $\{210\}$ tips (Figure 2c). It is worth pointing out that there are no $\langle 0001 \rangle$ -oriented WZ InP NWs or $\langle 111 \rangle$ -oriented ZB InP NWs observed, although these specific directions are the most common NW growth orientations obtained for the Au-catalyzed VLS-grown NWs. The detailed explanation of this phenomenon will be discussed in the later sections. In short, by adopting the $\langle 210 \rangle$ -orientated PdIn solid alloy catalyst seeds, the as-prepared InP NWs possess excellent crystallinity and superior electron mobility with nonpolar growth orientations as well as minimized defect concentrations.

At the same time, it is also critical to understand the detailed relationships among the NW growth characteristics, the uniform NW orientation and the excellent NW crystallinity. As summarized in Table 2, the surface energies of different

Table 2. Surface Energies of PdIn Catalyst Seeds with Different Exposed Surface Planes

PdIn	surface energy (keV)
{001}	1.1197
{110}	0.8242
{111}	0.9325

crystal planes of the polyhedral-shaped PdIn catalyst seed are computed. Since PdIn has a body-centered cubic (bcc) crystal phase, its {110} planes are anticipated to have the highest atomic packing density, resulting in the lowest surface energy. In this case, the solid-state PdIn catalyst would thermodynamically prefer to adopt a hexagonal-shaped configuration exposing the lowest surface energy {110} planes. In addition, during the NW nucleation, when the In constituent first precipitates from the PdIn catalyst and then reacts with the P precursor vapor to form InP NW segments, the minimized lattice mismatch at the NW catalyst/body interface would predominantly dictate the NW growth here. In this lattice-matching relationship, the PdIn{110} planes exhibit a relatively large lattice mismatch of >10% against ZB InP {111}, {110} and WZ InP {0001} planes as illustrated in Figure 3, Figure S4, and Table 3. As a result, there is a minimum number of InP NWs growing along the ZB <111> or WZ <0001> directions. In contrast, the PdIn {210} planes have a reduced lattice mismatch of <5% against WZ InP {2110} planes, in which the corresponding interface free energy is minimized, facilitating the effective NW growth with the seed/body interface relationship of PdIn {210} | InP {2110}. In the meanwhile, there is also a small amount (<10%) of WZ InP {1100} NWs observed due to the slightly larger in-plane lattice mismatch at the PdIn {110}/WZ InP {1100} interface as

compared to the one of PdIn {110}/InP {2110}. These {2110} and {1100} orientations are nonpolar in wurtzite InP NWs as compared with typically observed polar <0001> orientation.^{20,47–52} It should be noted that this in-plane lattice matching phenomenon contribute to the efficient NW growth with the excellent crystallinity and minimized defects *via* VSS mode as depicted in Figure 2b,c as compared with the commonly observed defective Au-catalyzed VLS grown InP NWs along ZB <111> and WZ <0001> directions. All these characteristics are also in good accordance with the previously reported Ni-catalyzed GaAs NW⁴⁰ and Pd-catalyzed GaSb NW growth.²⁸

Moreover, the atomic stacking is as well modeled to compare the intrinsic stacking difference of InP NWs growing along different orientations. As demonstrated in Figure 3b,c, the atomic arrangements of first In layers of InP ZB {111} and WZ {0001} are the same, while the top [PIn₃] groups have different in-plane rotations. If the top layer of In atoms lie in the hollow site, the stacking sequence would turn into “abcabc”, yielding the ZB structure. If the top layer of In atoms lie on top of the preceding layer of P atoms, the stacking sequence will be “abab” contributing to the WZ structure. Notably, since each In atom in the first layer has only one bond linked to the top [PIn₃] layer, the easy spatial rotation would always lead to the mixed stacking, which generates a high concentration of stacking faults typically observed in InP NWs reported in the literature. However, as depicted in Figure 3e and Figure S4c, when the In and P atoms configure in the nonpolar WZ {2110} and {1100} planes, the top layer of each In (P) atom would have one bond linked to the preceding layer P (In) atoms, 1–2 bonds linked in-plane with P (In) atoms, and the other 1–2 bonds linked to the layer P (In) atoms above; therefore, the bond rotation is strictly prohibited there, yielding a minimized concentration of stacking faults and other related defects. This way, the appropriate lattice matching would not only induce the InP NWs growing along the nonpolar directions with enhanced crystal quality for advanced electronic and optoelectronic application, but also

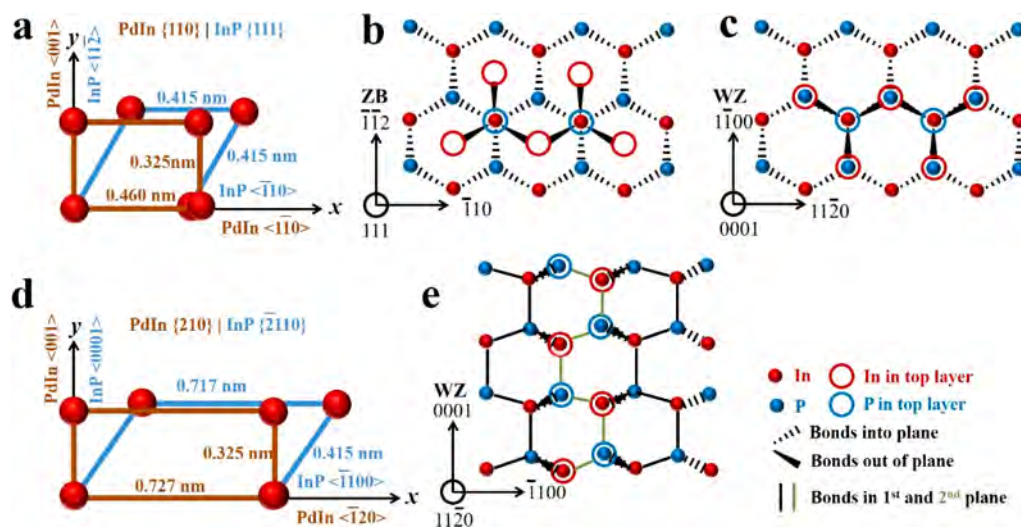


Figure 3. Schematic illustration of the proposed atomic modeling. In-plane In atom alignments of the catalytic seed/NW interfaces of (a) ZB PdIn {210} | ZB InP {111} and (d) ZB PdIn {210} | WZ InP {2110} showing the minimal lattice mismatch between ZB PdIn {210} and WZ InP {2110}. Atomic stacking in (b) ZB InP {111}, (c) WZ InP {0001}, and (e) WZ InP {1120} NW orientations, showing no bond rotation is allowed in WZ InP {1120}; therefore, no stacking fault is resulted as compared with the easily rotated In–P bond, leading to the transformation between ZB <111> and WZ <0001>.

Table 3. Calculation and Comparison of the Lattice Mismatch (%)^{a,b}

catalyst seeds	NW body							
	WZ InP {2110}		WZ InP {1100}		ZB InP {110}		ZB InP {111}, WZ InP {0001}	
	x-axis	y-axis	x-axis	y-axis	x-axis	y-axis	x-axis	y-axis
PdIn {210}	-1.4	4.4	-6.9	21.5	-23.9	21.7	-75.2	9.6
PdIn {110}	35.8	4.4	32.3	21.5	21.6	21.7	-10.8	9.6
PdIn {111}	35.8	-17.2	32.3	3.8	21.6	4.0	-10.8	-10.9
PdIn {100}	54.7	9.5	21.5	52.2	21.7	44.6	21.7	9.6

^aNote: Lattice mismatch can be calculated by the equation of $[(a_{\text{NW}} - a_{\text{Cat}})/a_{\text{NW}} \times 100\%]$, where “a” represents the lattice constant of each described species. ^bThe In atom alignment difference between the PdIn catalyst seed and the InP NW existed in both WZ and ZB structures.

suppress the NWs growing in the ZB phase or along other directions with the larger lattice mismatch and higher interfacial energy.

To further evaluate the role of nonpolar orientations on the obtained high electron mobility of InP NWs, the relationship among electron mobility, effective mass (m^*) and scattering time (t) should be considered in the analytical equation of $\mu = et/m^*$, where e is the electron charge.⁵³ It has been noticed that although the effective masses of electron are somewhat different in the parallel (m_{\parallel}^*) and perpendicular (m_{\perp}^*) directions to {0001} orientations due to the anisotropic property of WZ InP crystal, the difference is still relatively small, where m_{\parallel}^* and m_{\perp}^* are found to be $0.078m_0$ and $0.093m_0$, respectively (m_0 is the electron mass in vacuum).^{54–57} The electron mass in {1010} and {2110} planes can also be determined as $m_{\parallel,\perp}^* = (m_{\parallel}^* m_{\perp}^*)^{1/2} = 0.085m_0$.^{54–57} As a result, the theoretical effective masses and mobilities of electrons transporting in polar and nonpolar wurtzite InP planes are quite similar. Even though there is always an built-in electric field existed in the polar materials, such as III-nitrides semiconductors and perovskites of $\text{CH}_3\text{NH}_3\text{PbI}_3$, resulting in a kind of acoustic phonon scattering,^{58–60} the scattering time of carriers would become slightly longer in the nonpolar materials. Furthermore, due to the almost defect-free crystal structure obtained in nonpolar-orientated InP NWs as compared with the defective polar-orientated ones, the scattering times in different NW orientations would vary greatly, in which the long scattering time associated with these defect-free NWs can account for the record-high electron mobility obtained, approaching the theoretical limit of InP NWs.

Apart from the NW crystallinity, it is essential to evaluate the potency of our Pd-catalyzed InP NWs for low-power and high-frequency electronics. Here, the top-gate NWFET is constructed with the corresponding SEM image and illustrative device schematic presented in Figure 4a. To be specific, the device is configured with the Pd-catalyzed InP NW as the channel, Ni electrodes as source/drain contacts and Ni top-gate. Al_2O_3 is employed as a high- κ dielectric, which is deposited uniformly onto the back-gated device channel by an industrial-friendly process of e-beam evaporation followed by low-temperature annealing. As shown in the $I_{\text{DS}} - V_{\text{DS}}$ curve in Figure 4b, the ohmic-like contact formation between the NW channel and Ni electrodes can be confirmed, being similar to the one observed in back-gated NWFETs. Based on the transfer characteristics depicted in Figure 4c, the device exhibits the typical n-type behavior with a small hysteresis at both $V_{\text{DS}} = 0.1$ and 0.4 V. Impressively, there is an extremely small OFF current ($I_{\text{OFF}} = 16$ pA) with $V_{\text{GS}} = -0.37$ V, and an ON current of ~ 385 nA with $V_{\text{GS}} = 1$ V, delivering an excellent

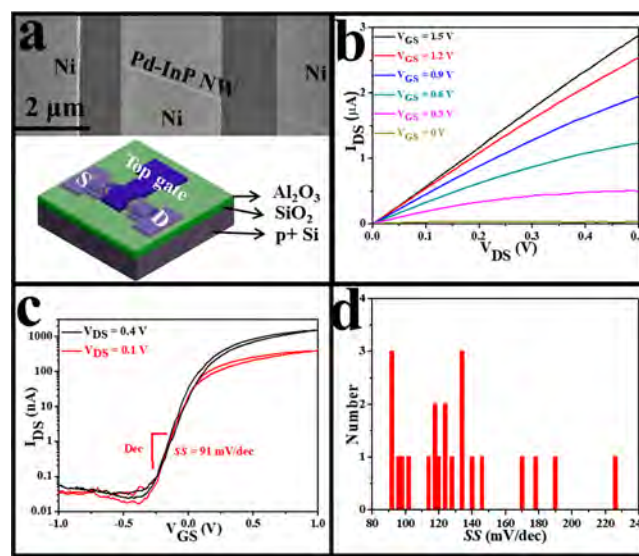


Figure 4. Electrical characterization of top-gated InP NWFETs. (a) Typical SEM image (top) and corresponding device schematic (bottom) constructed with Ni metal electrodes, Ni top-gate, and Pd-catalyzed InP NW channel. (b, c) Output and transfer curves of the representative device, respectively. (d) Subthreshold slope (SS) statistics of compiling more than 20 devices.

$I_{\text{ON}}/I_{\text{OFF}}$ ratio of $\sim 2.4 \times 10^5$ at room temperature. In the meanwhile, the electron mobility is also estimated to be >1300 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ with details as shown in Figure S5, where the findings are perfectly consistent with the ones calculated for the back-gated NWFETs. In any case, there may be a relatively small variation in these mobility values, which might be attributed to the errors in the capacitance simulation of Al_2O_3 since the Al_2O_3 thin film may not necessarily envelop the InP NW conformally as described in the model (Figure S5). As shown in Figure 4c, the subthreshold slope (SS) of the as-fabricated top-gated NWFET gives a respectable SS of 91 mV dec^{-1} with $V_{\text{DS}} = 0.1$ V at room temperature, which is close to the theoretical limit of 60 mV dec^{-1} . In the low-power and high-speed operations, this important parameter of SS is defined as $dV_{\text{GS}}/d \log I_{\text{DS}}$, which evaluates how efficient a FET can be switched on and off. In other words, a smaller SS value indicates a faster transition between the device ON and OFF states. Here, the SS value of 91 mV dec^{-1} is even smaller than the recently reported values ($95, 108, 157, 200$ mV dec^{-1}) of many wrap-gated NWFETs.^{61–64} In any case, many of the SS values are below 200 mV dec^{-1} with $V_{\text{DS}} = 0.1$ V as shown in the statistics in Figure 4d, indicating the reduced electron scattering at the interface between NW channels and e-beam evaporated gate dielectrics. These steep subthreshold slopes

and good capacitive gate coupling of the top-gated devices can clearly infer the excellent crystallinity of our InP NWs grown along nonpolar directions, suggesting their technological potential for future high-frequency electronics with low-power dissipation.

Furthermore, since InP is also an ideal active material for optoelectronics because of its appropriate direct bandgap, the photoresponse of InP NW devices are hence evaluated in details here. Based on the transfer and output curves measured in dark and under light illumination (Figure 5a and b), it is

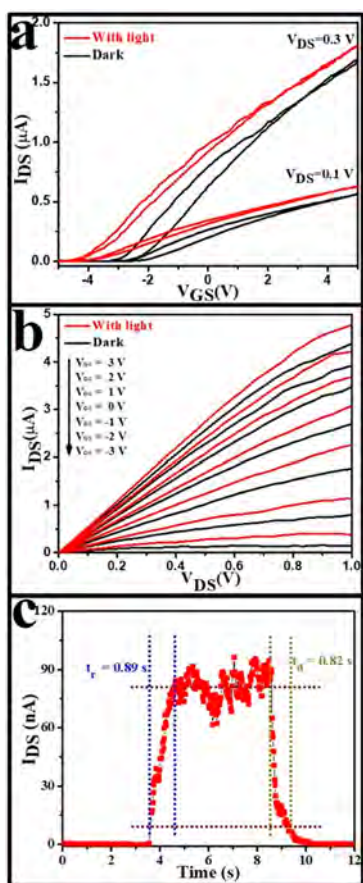


Figure 5. Photodetection performance of InP NWFETs. (a) Transfer and (b) output characteristics of the representative device measured in dark and under light illumination. (c) High-resolution response/recovery curve of the detector device at $V_{ds} = 0.1$ V and $V_{gs} = -3$ V. The incident wavelength and light intensity are 532 nm and 20 mW cm^{-2} , respectively.

noticed that the output current increases greatly under the light illumination, indicating their photosensing properties of InP NWs. In order to assess the stability of fabricated NW detectors, the output current is as well measured with prolonged time under the chopped light (Figure S6). Explicitly, the obvious ON and OFF states with an ON/OFF current ratio of 1.2×10^3 as well as the good stability can be observed when the light illumination is modulated. In this case, the photoresponsivity can be estimated as $\sim 10^4 \text{ A W}^{-1}$, which is already one of the highest responsivities among all InP NWs reported in the literature,^{3,65,66} demonstrating again the advantage of our high-quality Pd-catalyzed InP NWs synthesized *via* VSS mode. In addition to the responsivity, a high-resolution current *versus* time curve is also collected to determine the response time of NW detectors (Figure 5c). The rise time is generally defined as the time for the current to rise from 10% to 90% of the maximum value and *vice versa* for the decay time.⁶⁷ Thus, the rise and decay times are found to be 0.89 and 0.82 s, respectively. In other words, as demonstrated in Figure 5 and Table 4, the as-prepared InP NW photodetector shows the advantages of high responsivity, high I_{ON}/I_{OFF} ratio, low dark current, and tunable photo-current *via* varying gate voltages. The relatively slow response times may be possibly due to the large amounts of surface states associated with the thin InP NWs here,^{68–71} in which their surface states can then act as the carrier traps. Controlling the surface-state concentration will be useful to further enhance the response time of InP NW photodetectors. All these findings evidently illustrate the technological potency of our InP NWs grown in nonpolar orientations for high-performance optoelectronics.

CONCLUSIONS

In summary, single-crystalline InP NWs along nonpolar wurtzite orientations have been successfully achieved by utilizing Pd catalysts *via* vapor–solid–solid growth. In specific, the PdIn seed/InP NW interface plane epitaxial relationship is found to play a key role in dictating the growth orientations, which is independent of the NW diameters and growth conditions. More importantly, when fabricated into InP back-gated NWFETs, the high electron mobility of approximately $2000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ as well as the high photoresponsivity of 10^4 A W^{-1} are obtained, attributable to the minimized crystal defects and the nonpolar growth orientation of InP NWs. Once the top-gated device geometry is employed, low subthreshold slopes of down to 91 mV dec^{-1} are resulted. The findings explicitly demonstrate the prospects of the single crystalline and high electron mobility InP NWs as good active

Table 4. Performance Comparison of Different InP NW Photodetectors

materials	growth method ^a	incident wavelength (nm)	operating temp (K)	responsivity (A W^{-1})	response time	recovery time	ref
InP NW	MOCVD	532	rt	6.8			66
InP NW	CVD	500–1200	rt	2.8×10^5	29.1 ms	139.6 ms	4
InP NW/InAsP QDs	MOVPE	827 and 532	10		175 ps	1.5 ns	72
InP NW	thermal evaporation	633	rt	779.14	0.1 s	0.46 s	65
N-doped InP NW	CVD		rt	1900	0.156 s	5.560 s	73
InP NW	CVD	532	rt	10^4	0.89 s	0.82 s	this work

^aMOCVD = metal–organic chemical vapor deposition; rt = room temperature; QDs = quantum dots; CVD = chemical vapor deposition; MOVPE = metal–organic vapor-phase epitaxy.

material candidates for applications in future high-speed, low-power, high-frequency electronic and optoelectronic devices.

METHODS

High-Performance InP NW Synthesis. A high melting temperature metal catalyst of Pd is adopted for the growth of InP NWs. The InP NWs are prepared by using a previously reported solid-source CVD method.²⁸ Specifically, in a dual-zone horizontal tube furnace, a solid source of InP powder (99.999% purity) is placed in the upstream zone and the growth substrate (Si/SiO₂ substrates) with 0.5 nm Pd catalyst film is located in the downstream zone. The distance between InP powder and growth substrate is 15 cm. Before the NW growth, a mechanical pump is used to create a vacuum of the growth chamber, and the corresponding pressure of the furnace goes down to 3×10^{-3} Torr in ~ 10 min. Then the growth system is purged with 100 sccm H₂ (the pressure of quartz tube is about 0.41 Torr) for 0.5 h. For NW growth, the upstream zone is heated to 710 °C in 8 min, and the downstream zone is heated to 710 °C in 7 min. After the NW growth, the dual-zone horizontal tube furnace is turned off, and the quartz tube is cooled to room temperature with the flow of hydrogen.

Material Characterization. SEM (Nova NanoSEM 450, FEI Company) and TEM (FEI TECNAI 20) are used to examine the morphology of the as-synthesized InP NWs. The microstructure and composition of the InP NWs are studied by HRTEM (JEOL 2100F, JEOL Co., Ltd., Tokyo, Japan) and associated EDS.

FET Fabrication and Corresponding Photoelectrical Property Measurement. For the fabrication of back-gated NWFETs, the as-prepared InP NWs are first dispersed in ethanol solution by ultrasonication and then drop-casted onto highly doped p-type Si substrates with a 50 nm thick SiO₂ layer. Then the source and drain regions are defined by photolithography. Ni films with 60 nm thickness are next deposited as contact electrodes by e-beam evaporation. After the lift-off process, the electrical and photoelectrical performances of the as-fabricated InP back-gated NWFETs are characterized by an Agilent 4155C semiconductor analyzer (Agilent Technologies, California) connected to a standard probe station. For photodetection performance measurement, the light wavelength and the light intensity are 532 nm and 20 mW cm⁻², respectively. The top-gated NWFETs are fabricated on the obtained back-gated NWFETs. In particular, after the fabrication of back-gated NWFETs, a dielectric layer of Al₂O₃ with 13.5 nm thickness was thermally evaporated, followed by a 10 h annealing at 100 °C in ambient for densification. The top gate regions are defined by a second photolithography process followed by a Ni electrode thermal deposition with a thickness of 60 nm. After the lift-off process, the Agilent 4155C semiconductor analyzer is used to measure the electrical performance of the fabricated top-gated FET.

Simulation Method. In our calculations, the diamond structure of the 64-atom Pd_xIn_y supercell is first constructed. It is important to note that the Pd and In atoms are randomly distributed according to experimental composition. Then the constructed models are optimized until all forces on the free ions converge to 0.01 eV/Å using the Vienna *ab initio* simulation package.^{74,75} The vacuum space is about 15 Å to consider the surface structure, which can be used to eliminate the interaction between periodical images. The Monkhorst–Pack *k*-point meshes are set as $4 \times 5 \times 1$, $4 \times 5 \times 1$, $4 \times 4 \times 1$, and $4 \times 4 \times 1$ for (110), (211), (001), and (111) surfaces, and 500 eV is set as the kinetic energy cutoff for the plane-wave basis, respectively. The surface energies are then calculated based on the following equation⁷⁶

$$\gamma_s = (E_s - E_b)/2A$$

where E_s and A are the energy and area of the surface, respectively, while E_b is the bulk energy without surface.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.8b05947.

Morphology and diameter distribution characterization of as-prepared InP NWs; transfer characteristics and gate oxide capacitance (C_{ox}) simulation of the typical back-gated FET using Pd-catalyzed InP NW as the channel; determination of the catalyst orientation with electron microscopy; schematic view of the atomic modeling; capacitance measurement, gate oxide capacitance (C_{ox}) simulation, device schematic, and peak mobility of the top-gated FET fabricated with the Pd-catalyzed InP NW channel (as shown in Figure 4a); current as a function of time under chopped light illumination performed in this study (PDF)

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Notes

The authors declare no competing financial interest.

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